Register No : _____

THE KAVERY ENGINEERING COLLEGE

(An Autonomous Institution)

B.E/B.TECH DEGREE END SEMESTER THEORY EXAMINATIONS, NOV /DEC 2024

Sixth Semester

Electronics and Communication Engineering

CEC334–Analog IC Design

Regulations – 2021

Duration : 3 Hrs *Maximum : 100 Marks*

*PART – A (ANSWER ALL QUESTIONS) (Marks 10*2=20)*

Q.No	*Questions*	*BLT*	*CO*	*Marks*
1.	Sketch the equivalent circuit of source follower.	RE	1	2
2.	Summarize the design challenges in creating high gain amplifier structure.	UN	1	2
3.	What is the Miller effect and how does it influence amplifier design?	RE	2	2
4.	List the statistical characteristics of noise relevant to electronic amplifiers.	AP	2	2
5.	Summarize the properties of negative feedback circuits.	UN	3	2
6.	Point out different types of noise in Op Amp.	AP	3	2
7.	Define phase margin and its significance.	UN	4	2
8.	Choose some alternative compensation techniques used in operational amplifiers.	AP	4	2
9.	Illustrate the common types of faults that can occur in digital circuits.	UN	5	2
10.	Compare Sensitive Scan Design and Partial Scan design.	AP	5	2

*PART – B (ANSWER ALL QUESTIONS) (Marks 5*13 = 65)*

Q.No		*Questions*	*BLT*	*CO*	*Marks*
11.	a	Using the small-signal model, analyze the voltage gain of a differential amplifier with an active load.	AN	1	13
		Or			
	b	Analyze the voltage gain and bandwidth of a cascode amplifier.	AN	1	13
12.	a	Analyze the frequency response of a Source Follower amplifier and determine its cutoff frequency.	AN	2	13
		Or			
	b	Using statistical noise models, inspect the noise performance of a single-stage amplifier.	AN	2	13

13.	a	i	Explain how negative feedback affects gain stability.	UN	3	7
		ii	Explain the way of minimize the effects of loading in feedback circuits.	UN	3	6
			Or			
	b	i	Explain how negative feedback can be applied in single-stage op-amps.	UN	3	7
		ii	Explain how to extend the input range using additional circuit elements.	UN	3	6
14.	a		Explain the different types Frequency compensation techniques with net diagram and necessary equations.	EV	4	13
			Or			
	b		Explain the techniques to improve the slew rate in two-stage op-amps	EV	4	13
15.	a		Compile the application of Ad hoc techniques to improve fault detection in a given circuit.	CR	5	13
			Or			
	b		Design a simple logic circuit and propose a method for level-sensitive scan design.	CR	5	13

*PART – C (Marks 1*15 = 15)*

Q.No			*Questions*	*BLT*	*CO*	*Marks*
16.	a	i	Analyze how built-in self-test can be integrated into a digital system design.	AN	4	8
		ii	Compare and contrast level-sensitive scan design and edge-sensitive scan design.	AN	4	7
			Or			
	b		Assess the role of fault simulation in validating fault detection techniques.	EV	5	15